memory 4 to the error detector 7.

Step (a-12): the error detector 7 performs error detection for the data transferred, and transmits the error detection signal 21 to the system control unit 1 in order to inform whether an error has been detected or not.

Through these steps, the horizontal error correction for one sector is complete.

In the same manner, horizontal error correction is executed for the subsequent 15 sectors including the outer code parity unit so as to complete the horizontal error correction for one block. If no error is detected from all sectors, the error correcting operation is complete; if there is an error detected even from one sector, the next process including vertical error correction will be executed.

The above-described prior art method, however, takes much time in a series of operations: the syndrome calculation by the syndrome calculator 5, the error correction by the error corrector 6, and the error detection by the error detector 7 done in this order. Above all, it is time-consuming to access the buffer memory 4 as storing means and to read data therefrom repeatedly because these operations are not performed like electric circuit but often mechanically done by relative movement between the readout means and the buffer memory 4.

Furthermore, a significant improvement in accuracy of reading and writing digital data to and from CD-Rs and other similar media in recent years has reduced the necessity of error correction by the error corrector. Nevertheless, the data in the head portions, which have been checked to contain no error, are often subjected to error detection by the error detector.

Consequently, error correction and error detection, which could be processed in parallel in most cases, are processed separately in time, thereby wasting much time.

The error correction and the error detection are not satisfactory in consideration of probable higher densities and more rapid readout of DVDs and other recording media in the future.

In high-speed reproduction performed to check the position of specific image data or to inspect their contents, it is not always necessary to reproduce image data completely. On the other hand, it is usually necessary for data relating to the programs of the CPU to be reproduced in a perfect form even if it takes much time. Thus, error correction must be performed at different levels, which have not been satisfactorily done so far.

Hence, it has been expected to develop an error correction device which performs error correction more accurately and faster in accordance with required performance levels.

SUMMARY OF THE INVENTION

The present invention has been contrived to solve the aforementioned problems by paying attention to the following: (1) the data of code words up to and including the code word subjected to error correction do not change in the error correction by the error corrector; (2) as a result of (1), the efficiency of the transfer of these data to the error detector can be improved; (3) the error rate; and (4) the data amount of each code word. To be more specific, the present invention has the following structure.

The aspect 1 relates to an error correction device comprising: a buffer memory for storing at least one sector of data (recording data in such a manner as to be able to be read or overwritten) having a structure where each of N words (strings) of error correcting code comprises a data unit including original image or audio data (main data) etc., an inner code parity unit, and one error detecting code (data transfer between actual units are usually done one ECC at a time, but the processes in the present aspect can be done one sector at a time); a syndrome calculating means for generating the syndrome for error-contained data read from the buffer memory; an error correcting means for correcting error-containing data in the buffer memory by detecting an error position from the syndrome generated by the syndrome calculating means and by calculating an error value; an error detecting means for detecting an error in error-corrected data generated by the error correcting means; a storing means composed of a register with a high-speed writing and reading ability so as to store mid-term results of an error detecting process in the error detecting means; a bus control means for controlling data transfer between the buffer memory, the syndrome calculating means, the error correcting means, and the error detecting means (preventing a collision between the units in reading, overwriting and other processes); and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times.

The bus control means transfers data from the buffer memory to the syndrome calculating means and to the error detecting means concurrently in code word units until the syndrome calculating means detects an